CLAIM AMENDMENTS:

Please amend the claims as follows:

1. (Currently Amended) A flash ROM management apparatus, comprising:

a storage device capable of storing a plurality of address records, each address record comprising an identity and an address range associated with ~~a flash ROM~~ one of a plurality of flash ROMs;

a strapping component, configured to output a signal ~~to determine flash ROM type~~ indicating one of a plurality of flash ROM types corresponding to the flash ROMs; and

a process unit, coupled to the storage device and the strapping component, receiving a memory access request with an access range from[[the]] a CPU[[and]], receiving the signal, determining the indicated flash ROM type according to the signal, querying the identity by matching the access range and ~~the address range~~ one of the address ranges in the address records, and executing an LPC 1.1 memory access instruction with the identity and the access range corresponding to[[the]] a memory cycle.

2. (Currently Amended) The apparatus as claimed in claim 1 wherein the identity is an "IDSEL" number associated with ~~a firmware hub flash ROM~~ one of a plurality of firmware hub flash ROMs.

3. (Original) The apparatus as claimed in claim 1 wherein the address range is a pair comprising a base address and an end address.

4. (Original) The apparatus as claimed in claim 1 wherein the address range is a pair comprising a base address and memory size.

5. (Original) The apparatus as claimed in claim 1 wherein the flash ROM type is an LPC flash ROM or a firmware hub flash ROM.

6. (Original) The apparatus as claimed in claim 1 wherein the memory access request is a memory read request or a memory write request.

7. (Currently Amended) The apparatus as claimed in claim 1 wherein, in the process unit, the LPC 1.1 memory access instruction is an LPC memory read instruction or an LPC memory write instruction, and the LPC memory read instruction or the LPC memory write instruction corresponds to[[the]] a LPC memory cycle.

8. (Currently Amended) The apparatus as claimed in claim 1 wherein, in the process unit, the LPC 1.1 memory access instruction is a firmware hub memory read instruction or a firmware hub memory write instruction, and the

firmware hub memory read instruction or the firmware hub memory write instruction corresponds to[[the]] a firmware hub memory cycle.

9. (Currently Amended) The apparatus as claimed in claim 1 wherein a basic input/output system (BIOS) flag within each ~~the~~ address record indicates whether the system BIOS is stored in flash ROM.

10. (Original) The apparatus as claimed in claim 9 further comprising a configuration unit detecting an error message indicating system BIOS failure, and resetting the BIOS flag for further reboot.

11. (Currently Amended) A method of flash ROM management, comprising using a computer to perform the steps of:

receiving a memory access request with an access range from a CPU;

receiving a signal indicating one of a plurality of flash ROM types corresponding to a plurality of flash ROMs output from a strapping component ~~to determine flash ROM type~~;

inputting a plurality of address records ~~associated with a flash ROM~~, wherein[[the]] each address record comprises an identity and an address range associated with one of a plurality of flash ROMs;

querying the identity by matching the access range and ~~the address range~~ one of the address ranges in the address records; and

executing an LPC 1.1 memory access instruction with the access range and identity corresponding to[[the]] a memory cycle.

12. (Original) The method as claimed in claim 11, wherein the memory access request is a memory read request or a memory write request.

13. (Cancelled)

14. (Currently Amended) The method as claimed in claim 11, wherein the identity is an "IDSEL" number associated with ~~a firmware hub flash ROM~~ one of a plurality of firmware hub flash ROMs.

15. (Original) The method as claimed in claim 11, wherein the address range is a pair comprising a base address and end address.

16. (Original) The method as claimed in claim 11, wherein the address range is a pair comprising a base address and memory size.

17. (Original) The method as claimed in claim 11, wherein, in the step of executing an LPC 1.1 memory access instruction with the access range and the identity corresponding to memory cycle, the LPC 1.1 memory access

instruction is an LPC memory read instruction or an LPC memory write instruction corresponding to LPC memory cycle.

18. (Original) The method as claimed in claim 11, wherein, in the step of executing an LPC 1.1 memory access instruction with the access range and the identity corresponding to memory cycle, the LPC 1.1 memory access instruction is a firmware hub memory read instruction or a firmware hub memory write instruction corresponding to the firmware hub memory cycle.

19. (New) The method as claimed in claim 11, wherein the signal is received before conducting power on self test (POST) procedure.

20. (New) A flash ROM management apparatus, comprising:

at least one flash ROM corresponding to one of a plurality of flash ROM types;

a strapping component, configured to output a signal indicating the flash ROM type corresponding to the flash ROM before conducting power on self test (POST) procedure; and

a process unit, coupled to the flash ROM and the strapping component, receiving a memory access request with an access range from the a CPU, receiving the signal, acquiring the flash ROM type according to the signal, and

executing an LPC 1.1 memory access instruction with the access range corresponding to a memory cycle corresponding to the flash ROM type.

21. (New) The apparatus as claimed in claim 20, wherein the flash ROM types comprise an LPC flash ROM and a firmware hub flash ROM.